

ABSTRACT OF THE DISCLOSURE

In a semiconductor device for generating complementary PWM signals for, for example, controlling an inverter, a dead time is flexibly added by using a simple architecture. A dead time addition unit adds time elapsing until a value of a timer reaches
5 a set value of a register as a first dead time at a rise of a first PWM signal. On the other hand, time elapsing until the value of the timer reaches a set value of another register is added as a second dead time at a rise of a second PWM signal.